



Chip Shots

Tom Cheyney's Semiconductor, Microelectronics, and Nanotechnology Blog

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[Semicon wrap: Molecular Imprints continues to press forward](#)

Friday, July 27th, 2007

With a burst of caffeine-infused energy, I pushed through the final Semicon afternoon to hit my final meetings on the show floor. One of those meets involved [Molecular Imprints](#) (MII), a nanoimprint lithography (NIL) company that I've been covering for years and last met with at SPIE Advanced Lithography.

Mark Melliar-Smith, MII's CEO, stirred up a lot of discussion with his plenary session talk at SPIE. His speech was part of what might be looked back on as NIL's coming-out party. Not so much as a production-worthy-now alternative to immersion, double-patterning, and other litho schemes in favor, but as a legit contender to extreme ultraviolet litho (EUVL) for the 32-nm and more likely 22-nm CMOS process generations. Given the alternatives, more of the litho and chipmaking crowd is taking a fresh look at NIL.

Although there's a lot of defect, overlay, and template work that still needs to be done to get NIL ready for mainstream chipmaking, it compares favorably to EUVL's report card. But MII has made orders-of-magnitude progress on all fronts over the past six months or so with its step-and-flash imprint litho (S-FIL) approach. And in terms of cost, NIL looks extremely attractive compared to EUVL, with its tool price tags that might hit corporate wallets at somewhere between \$50 mill and \$100 mill a pop.

I met with Mark, CTO S.V. Sreenivasan, and marketing/biz dev VP John Doering, who filled me in on the latest developments at MII. Their three-pronged market strategy—CMOS semi, nanotech (hard disk drives, high-brightness LEDs) and future apps (CMOS image sensors, FPDs, biomed)—continues apace, with progress in all areas. Their roadmap reveals a tiered or staged approach to ramping volume manufacturing, starting with HB-LEDs in the 2008 timeframe, next-gen bit-patterned-media HDD in 2010, and volume CMOS NAND flash in 2011 or so.

But Mark told me that the pull of memory, specifically storage-class memory, may bring that 2011 date in. Recent IBM data from its storage-class memory work (that is, chips with memory capacities rivaling those of hard-disk media) show very promising sidewall profiles. He cited "excellent litho results at 30 nm," with average critical dimensions of 33.3 nm, CD variations of 3.5 nm 3 sigma, line-edge roughness

(LER) of 2.2 nm 3 sigma, and linewidth reduction (LWR) of 2.6 nm 3 sigma.

On a related note, MII's Imprio 250 tool that shipped earlier this year for unit-process development and device-prototyping applications at an Asian memory-chip customer (reported elsewhere to be Toshiba, but the MII guys would only smile when I asked them to confirm that) was installed and accepted at the fab in nine weeks, according to Mark. The patterned 300-mm wafer they proudly showed me during our meeting was printed on the tool at you-know-who's facility. A paper about you-know-who's work with MII's tool will be presented at this year's [International Conference on Micro- and Nano-Engineering \(MNE\)](#), taking place in Copenhagen in late September.

On the template front, MII has been working diligently with Japanese maskmakers and e-beam mask-writing tool suppliers. Mark says they're getting access to both NuFlare's 5000 and 6000 VSB e-beam systems, pushing capabilities toward 32-nm half-pitch. For 20 nm and below device prototypes, MII and its partners are also using Gaussian pattern-generating tools.

"Our tools are being used by customers for good and sufficient reasons," Mark noted. "We still have a long road to hoe, but we're making real progress." Added John, "we're making holes and pillars for [all kinds of] memory types, we're a 'density enabler' across the board," which echoed what S.V. had said a few minutes earlier: "We're about density, not feature size."

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[SEC's got its eyes, claws on Schroeder, Therrien](#)

Thursday, July 26th, 2007

Surprise, surprise! The Securities and Exchange Commission (SEC) has handed down stock options backdating-related indictments of two former semiconductor equipment company honchos: Ken Schroeder (ex-KLA-Tencor) and Robert Therrien (ex-Brooks Automation). Ken faces civil fraud charges, but avoided the ignominy of criminal counts, while Bob got hit with the double-shot of civil and criminal (for tax evasion).

First, here's a bit of what I pulled off [the Dow Jones Newswire account about Ken's](#) legal peccadillo:

"The SEC filed civil-fraud charges against Kenneth Schroeder, 61 years old, of Los Altos Hills, Calif., accusing him of repeatedly backdating options between 1999 and 2002. The SEC also said he backdated in 2005, after passage of the Sarbanes-Oxley Act limited backdating opportunities by requiring companies to disclose stock-options awards within two days."

Now here's some of what DJ had to say about [Bob's even-dicier predicament](#):

"Federal prosecutors on Thursday said that a grand jury has handed up a one-count criminal indictment accusing former CEO Robert Therrien, 72 years old, of tax evasion. Prosecutors allege that Therrien backdated an option to purchase 225,000 company shares after he learned that his options to buy the stock had expired months earlier, in August 1999."

"The Securities and Exchange Commission filed civil securities-fraud and other charges