Dr. S.V. Sreenivasan, CTO, Molecular Imprints

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S.V. Sreenivasan is a co-founder and the CTO of Molecular Imprints Inc. (Austin, Texas). He is on leave of absence from the University of Texas at Austin, where he is an associate professor of mechanical engineering and the Thornton Centennial Fellow in Engineering. He received his Ph.D. in mechanical engineering from Ohio State University . He specializes in the areas of nanofabrication processes and design of ultra-precision machine systems. His specific research interests include the study of nanoimprint lithography, micro and nano-precision machines, precision optical systems, and real-time sensing architectures. Molecular Imprints, founded in 2001, designs, develops, manufactures and supports nanoimprint lithography systems. These systems are capable of patterning nanoscale devices and structures.

S.V. Sreenivasan (Source: Molecular Imprints)

SI: *Over the past three years, the industry has experienced considerable change. How do you see the role of the CTO today?*

Sreenivasan: In our specific business, which is quite capital-intensive and expensive from an R&D perspective, my role requires not only to understand tool roadmaps, development and technology, but also to have the ability to form complex partnerships with a number of companies. One must also figure out ways in which to fund these partnerships and research activities. I started off as someone who understood the technology, but who now must take the leadership in forming what are essentially technical consortia to develop the technology.

SI: *So your role is not just a technology-oriented one — it also has a political facet.*

Sreenivasan: I am not sure that it is political, but it requires developing partnerships and building consensus. For example, we have a significant research effort that was funded by the NIST ATP program, which involves Photronics, KLA-Tencor, Motorola and others. We're also working with other companies on the template technology, including DuPont Photomasks and DNP in Japan. So it's really not the tool development, which we do as a company, but also all the other needed developments that go with our internal efforts to make this technology viable.

SI: *Aside from the joint efforts and partnerships, how big is Molecular Imprints' R&D effort?*

Sreenivasan: Depending on how you look at it, ~40% of our company is fully devoted to R&D — certainly half of our engineering and scientific staff is. There is considerable tool research, materials research and process development work taking place.

SI: *What is the focus of your R&D effort?*

Sreenivasan: As a tool manufacturer, we're expected to come up with tools that offer improved lithography performance. And lithography performance includes arriving at a process with an etch capability to produce 50 nm features with good CD control, good overlay for integrated devices, good throughput, and low process defectivity.

SI: *How would you describe you R&D philosophy?*

Sreenivasan: It's driven by an ongoing attempt to understand customers' requirements. The marketing exercise that we regularly do — which involves our marketing and sales people, as well as our technologists — is aimed at trying to get some consensus on what the customers' needs are in specific market segments, because each segment has very different requirements. Our challenge is to understand these key market segments and their requirements, and then internally try to have a program to develop the building blocks that will be needed to address these markets. Simultaneously, we must maximize the synergy between all these activities. The difficult part in all this is that, with limited resources, we must avoid becoming completely fragmented, which would make us unable to play in any market segment.

SI: *You are one of the original developers of step-and-flash imprint lithography, and Molecular Imprints is the largest single organization working solely on it. What can you tell us about this?*

Sreenivasan: The work was initially begun at the University of Texas, and I worked very closely with Grant Willson, who is well-known in lithography circles. I was then a professor of mechanical engineering. We began working on this project around 1996 and, because of my mechanical engineering background, I was involved in the tool-building activity in the early days, while Grant was developing the materials to support the process development. When we founded the company, it was clear to us that in the lithography area the first thing one needed was a tool manufacturer to promote the technology.

SI: *Why is that so?*

Sreenivasan: There are various ways in which to leverage a technology. Our approach was that we'd build the basic infrastructure that would enable device manufacturers to take advantage of this new nanolithography technology. We realized that, to do this, the first thing you need is the tool technology, so I found myself in the middle and had to make decisions on how to move it forward. After a number of discussions with industry leaders, we decided that trying to get a core group to develop the tool technology was critical, and I ended up founding the company and leading the effort.

SI: *How would you position your technology among all the others?*

Sreenivasan: There was some excellent early work done by Steven Chou and others in Princeton , which demonstrated the technology's resolution and showed its nanoscale promise. What we did as a team in those days was to look at it and ask ourselves how we could take it and turn it into a stepper technology that the industry would accept and use, with the critical issue being that they had to be able to use it in conjunction with the existing infrastructure. This, of course, is because people have considerable investment in existing photolithography and associated technologies.

SI: *Not an easy undertaking.*

Sreenivasan: Indeed not! In principle, we had to come up with a tool that would seamlessly fit into the scheme, and do perhaps just one level of lithography and mix-and-match with the rest of the infrastructure. When we started thinking about that, there were several issues regarding how this lithography technology would evolve — specifically things like overlay and defectivity. So we gravitated toward this low-viscosity imprint process, which is very gentle and requires no high pressures and temperatures. Today, the process is 0.25 psi and uses very low-viscosity liquids, which allows us to operate at room temperature and do very fine alignment and overlay. All along our thinking was to allow our tools to work with all the billions of dollars of fielded equipment. Our latest tool, for example, has the capability to do magnification correction, to mix-and-match with photolithography. We're unique in this respect.

SI: *By the nature of your product, you are deeply involved in nanofabrication: advanced packaging, data storage, MEMS and NEMS. How do you view nanotech's development, and which do you view as the most serious hurdles facing it?*

Sreenivasan: "Nanotechnology" is a very broad term, and much depends on how people perceive it — I have seen various definitions. What interests me is that, if you're able to manipulate things at the nanoscale, you can take advantage of new physical phenomena. This was impossible at a bigger scale. This leads to new products and applications, but at the same time, you want to simultaneously maintain the benefits that exist in microfabrication. For example, commercially there is no value in writing a small area using an e-beam and creating nanostructures, because the throughput is so low that it cannot be used to make any consumer product. Photolithography has allowed us to process things at such a high throughput, and with such great reliability and repeatability, that it has established a production leadership position.

We want to be able to do this at nanoscale dimensions and enable new applications based on that capability. So there are areas in optics and magnetic storage where, if you begin creating features in the 100 and 50 nm scale, you can leverage phenomena that cannot be used at larger scales. This could open numerous applications in displays, high-brightness LEDs, in ultrahigh-density magnetic storage for consumer applications. These are the things that excite us as a company. And there is always the big brass ring of silicon, so even if we can mix-and-match with existing photolithography but take on some critical levels, such as perhaps the contact level, we still bring value to the table.

SI: *It seems as if the industry has forever looked at the ITRS as the compass pointing to the future. How do you view it?*

Sreenivasan: On the positive side, it's an excellent venue for vendors and chip manufacturers to work together, at least in formulating nominal goals. It is very useful in that it provides general guidelines regarding how one might position one's technology and development efforts. When you're on the roadmap, it also motivates suppliers and others to continue moving a technology forward. Because it is a consensus-builder, the roadmap has limitations in that it averages the requirements of the several device sectors. For any technology to be successful, you cannot depend on averages because you, your customers and suppliers may need to have requirements that are quite different from those outlined in the roadmap. Plus there are variations on practically every specification when you consider the work being done by those involved in logic or memory. The roadmap can be helpful as a baseline, but you must do considerable work for the specific market segments.

SI: *There is no roadmap for nanotech.*

Sreenivasan: True. Our big challenge there is that things evolve rapidly and that there is no standard or standards set. This increases the risks that are associated with it. Then again, the new markets allow us to set some of these new standards — it's a great opportunity.

SI: *Speaking of which, how does your roadmap look for the next couple of years?*

Sreenivasan: Broadly, we're looking at emerging markets — nanotechnology-type applications and the silicon CMOS opportunity. In the emerging markets, we have key segments like optical devices and storage. We work closely with key customers in these areas, to realign our roadmap and meet their needs. To be successful as a company, we must be able to put things into production. In advanced lithography, which is more on the silicon side, we constantly consult with our key customers both in logic and memory sides to keep in line with their requirements. That being said, one must manage one's resources carefully — you cannot commit everything to the customer — so there's always a healthy tension between us and customers as to what we sign up for in our roadmap and how we deliver on these commitments.

SI: *You've mentioned the "silicon side." New materials and processes are now being introduced at a rate that would have seemed impossible not too long ago. As your company's CTO, how do* *you view and face this challenge?*

Sreenivasan: The increase in the rate of introduction that you mentioned is a positive for us, because we're a new technology, and the fact that people are facing unprecedented numbers of new technologies and are taking the risks to continue marching along the roadmap makes them more open to accepting our technology. On the downside, if, for example, we decide to insert our technology sometime down the road, say at the 45 nm node, we must understand what the rest of the industry will look like at that node, and that's not yet fully decided. For example, on the back end, dielectric materials are in a state of flux and there is much discussion regarding which kinds of materials will be used and what their properties will be.

We must keep in touch with all this to ensure that we'll be relevant when we get there. This is a great challenge, and to a large extent, we depend on our customers to help us with it; much of the new materials development is proprietary technology still being developed by the materials suppliers.

SI: *Obviously, your company must deal with a number of device manufacturers. What would you say is their greatest challenge?*

Sreenivasan: Lithography is always the big challenge, and things change rapidly. Two years ago we were trying to compare ourselves with 157 nm lithography — today it's immersion lithography. What we bring to the table is really dense-pitch lithography and the potential for 3-D printing. People in the optical lithography world are relaxing the pitch requirements — the way they define the nodes is no longer half-pitch. Yet, they need to pack more devices into the wafer. And 3-D printing (which optical lithography cannot do) could significantly impact device fabrication in the future.

SI: *If you didn't have to worry about resources, which problem would you like to tackle?*

Sreenivasan: Template inspection and repair. Among the greatest challenges we face in advanced lithography is defect and yield, because it requires us to put tools into the fab in order to fully understand it. The central question within defect is 1× template inspection and repair. We have ongoing efforts with KLA-Tencor, DuPont and others in the mask business to develop this infrastructure. This is challenging because of the way, historically, the mask industry has operated. There are far more resources devoted to solving problems on the wafer. Funding has never been abundant for solving mask problems.

SI: *Are there any trends we should be more aware of?*

Sreenivasan: Nanotechnology, certainly. In the short run, its applications may be smaller when compared to silicon's, and therefore not too exciting from a business viewpoint. However, as a technologist, I see new huge markets developing. It can have effects on things as basic as lighting your house or business, while decreasing power consumption, with huge economic and ecologic impacts. Storage is going to be revolutionized — there could be ultrahigh-density storage inside every iPod and cell phone, changing how consumer products are developed. Then, of course, there can also be many biological applications that are enabled by nanopatterning.