NANOTECHNOLOGY

small print

To make more powerful computer chips, researchers are developing nanoscale tools.

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The Cray 1 Supercomputer was a technological marvel in 1976, when it was first sold, and researchers who worked with complex models of the Earth's atmosphere or the dynamics of a nuclear explosion clamored to get access to one.

But that power didn't come cheap. A Cray computer could cost several million dollars and required 60 kilowatts of power to operate. The Cray 1 weighed some 5,300 pounds.

Over the generation since the first Crays appeared, a miraculous thing has happened—supercomputers are everywhere. A computer that can run circles around the Cray 1, which could only operate at 83 megahertz, now draws only a few watts and costs just a few hundred dollars.

Such progress has transformed the economy and culture in innumerable ways. But the methods by which this progress was achieved, advanced photolithography, is rapidly approaching some hard, fundamental barriers. Without a new technological direction, semiconductors and the devices that depend on them will stop becoming cheaper, lighter, and faster. What this would portend for the economy is hard to fathom.

Fortunately, there is a new approach that may take semiconductor technology to an even smaller level. This new approach promises to make semiconductor features that can be compared in size to individual molecules. Once this approach is in wide use, we may discover that today's PCs will become as antiquated as 1970s-era supercomputers.

The trend toward ever-smaller semiconductors was first noticed as long ago as 1965. That's when Intel's Gordon Moore, then the director of research at Fairchild Semiconductor, formulated what is now known as Moore's Law: The number of components that can fit on an integrated circuit doubles every 18 months to two years.

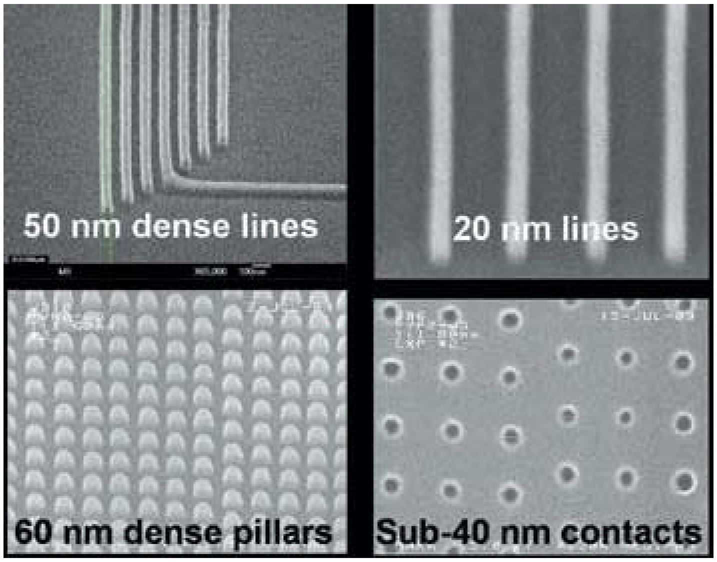
The trend has held up for four decades. The 1971 Intel 4004 chip had 2,250 transistors; the present-day Pentium 4 holds 42 million.

PROJECTING FEATURES

The key to this progress is microlithography, which in general terms is the process used to create micrometer or submicrometer scale structures for fabricating various kinds of devices, including integrated circuits, biochips, MEMS, and optical components. Since the 1960s, microlithography has been dominated by the use of light and photosensitive material to etch details onto a silicon substrate. In a sense, this photolithography can be thought of as a high-end projection camera that can cast the details of a circuit layer from a photomask to a photosensitive material on the wafer. While it can take a few hours to inscribe the photomask using a slow, serial process, photolithography allows for the nearly instantaneous parallel transfer of millions of pixels of data from the photomask to the wafer.

The use of progressively shorter-exposure wavelengths, along with an increased complexity in photomask design, has led to the reduction of the minimum feature size in photolithography.

Leading-edge photolithography now operates at a wavelength of 193 nanometers, or about 8-millionths of an inch. At this wavelength, pattern structures with a half-pitch as low as 90 nm can be etched. The continuous reduction in wavelength— research now is investigating extreme ultraviolet light at 13.2 nm— combined with highly sophisticated designs of lenses, mirrors, and masks, and with innovation in materials, processes, and machines will probably enable sub-70 nm lithography, and may even enable sub-50 nm lithography.



Imprint lithography has the potential to fabricate molecular-scale features. Lines only 50 and 20 nm wide (shown in micrographs, top left and top right), pillars 60 nm across (above left) and contacts just 40 nm wide (above right) were made with the S-FIL process. So far, the only limit on the scale of features produced has been the ability to make templates with fine enough features.

With shorter wavelengths, however, there are long lists of new and substantial technical challenges that lead to very expensive research and development programs and extremely high tool and mask costs.

In order to avoid going to shorter wavelengths, the industry has begun to develop 193 nm immersion lithography, wherein the lens and the scanning wafer are coupled by a liquid interface to increase the numerical aperture of the optics. But many key questions remain. It is not clear how high the tool cost will be, or what throughput will be. Only one polarization of light will be helped by immersion. Its impact on source design and the eventual lithographic performance are not fully understood. Also, it is believed that 193 nm immersion is not readily extendable beyond the 45 nm node.

Indeed, prohibitive costs, not actual physical limits, are likely to make the traditional approach of decreased wavelength impractical. Historically, the cost of optical exposure tools has increased exponentially. The cost of a single state-of-the-art, 193-nanometer tool approaches $20 million. This trend is projected to continue, with a single tool costing more than $50 million for sub-50 nm lithography.

In addition to the cost of the tool, the recurring and consumable costs associated with process materials, environmental control, complicated photomasks, and other factors will make next-generation lithography technologies a high-risk proposition. At these prices, the only way to recover these costs is to have high production volumes, long tool and photomask lives, and excellent process control.

LEAVING AN IMPRESSION

Photolithography may be running out of steam, but there are other approaches that potentially can step into the breach. While microlithography has been a top-down approach, relying on macroscale innovations, the unique physical and chemical phenomena at the nanoscale can lead to new techniques that can supplant photolithography. A low-cost technique derived from such an approach should not only enable making structures that are smaller than 50 nanometers, but it should also retain the overall benefits of photolithography.

Faced with these constraints, in the mid-1990s, several research groups in industry and academia started investigating "imprint lithography" methods for fabricating small features. Imprint lithography is essentially a micromolding process in which the topography of a template, or mold, defines the patterns created on a substrate. Investigations in the sub-50 nm regime indicate that imprint lithography has almost unlimited resolution.

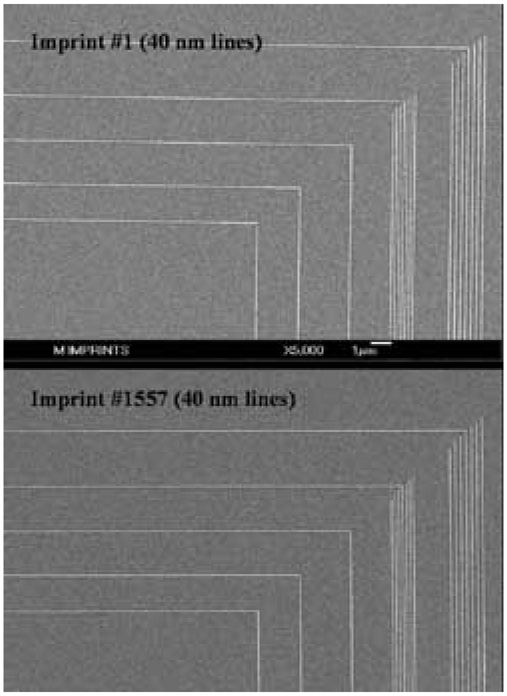
At the University of Texas, we developed a room temperature, very low pressure variant of imprint lithography known as Step and Flash Imprint Lithography, or S-FIL. The technology was licensed to Molecular Imprints Inc. for commercialization in 2001.

Step and Flash Imprint Lithography begins by spin-coating an organic layer onto a substrate. Then a low-viscosity, silicon-rich, UV photo-polymerizable imprint solution is dispensed on the wafer to form an etch barrier in the area to be imprinted. We then align a surface-treated, transparent template bearing patterned relief structures over the coated substrate. The template is lowered onto the substrate, thereby displacing the solution, filling the imprint field, and trapping the photo-polymerizable imprint solution in the template relief.

The quartz template is transparent, allowing for irradiation of the imprint solution with UV light through the backside of the template. After the solution has been cured, the template is then separated from the substrate, leaving an organo-silicon relief image on the surface of the coated substrate that is a replica of the template pattern. The wafer is then stepped and the process is repeated on the next field.

To date, our patterning resolution, about 20 nm, is limited only by the electron beam resolution of the template fabrication process. We have also demonstrated the replication of multitiered 3-D structures.

The S-FIL templates are made using the standard photomask fused silica substrates. The template is essentially a mask that is already used in advanced photolithography. It may seem that the photolithography mask has an inherent advantage over templates, since a typical photolithography process uses a factor of four reduction in its imaging. That is, the masks are four times bigger than the eventual features on the wafer. This apparent advantage does not exist due to a recent trend in photolithography, where the eventual features printed on the wafer are smaller than the wavelength of light. This requires the presence of "sub-resolution" features that are approaching 1X on the photomask.



Another promising aspect of S-FIL is its ability to produce thousands of defect-free impressions. In a test run of an S-FIL template that makes 40 nm wide features, the first imprint (top) is indistinguishable from imprint 1,557 (above).

The S-FIL process is specifically designed to address critical manufacturing issues, such as process defect control, precise overlay of multiple device levels, and the ability to pattern structures with arbitrary pattern density variations. The process uses ultra-low viscosity UV curable liquids to fill the template; this leads to a lithography process that operates at very low pressures—less than 0.25 pound per square inch.

The low-pressure environment contributes to a relatively long template life and a low number of process defects. (To date, we have been able to replicate 1,500 imprints—equivalent to about fifty 200 mm wafers—without degradation in sub-50 nm features.) We can also process fragile substrates, such as gallium arsenide and indium phosphide.

The low-viscosity liquid interface means that the template can slide on the wafer to within nanoscale accuracy, enabling very precise *in-situ* overlay capability. It is believed that this technique can be extended even further, to obtain alignment corrections of a few nanometers.

Because S-FIL uses a transparent fused silica template, the technique enables the photocuring process to occur while the template is in place and also allows for optical alignment of the wafer and template. The process also uses "drop-on-demand" fluid delivery that can be tailored to fabricate device geometries that have arbitrary pattern densities.

As a result, we have found that S-FIL can meet the stringent requirements of volume fabrication of nanoscale devices. For example, Molecular Imprints developed a commercial imprint lithography stepper that can be used for process development and nanoscale device prototyping. Due to the absence of complicated optics, these steppers cost a fraction of high-end optical lithography tools, while allowing the patterning of much smaller features.

MAKING IT SMALL

Lithography tools have been called the milling machines of the 21st century. They have revolutionized the electronics industry and are continuing to enable many applications at the micro- and nanoscales. The S-FIL process can cost-effectively fabricate sub-50 nm structures, complicated patterns, and 3-D structures, while it provides precise overlay and low process defectivity.

Such a technology will most likely address key market segments, such as optical devices, microdisplays, and nanoscale electronics. The impact of this technology on mainstream silicon fabrication will probably be a direct function of how well a key manufacturing challenge can be overcome: minimizing long-term defects both in the S-FIL process and the template fabrication process to maximize yield. The future challenge is to develop and demonstrate an S-FIL process that can approach the long-term yield and productivity of photolithography.

In the long term, imprint lithography or some other non-optical nanoscale fabrication technique promises to bring the first fruits of nanotechnology. Once such fabrication becomes routine, we will see the commercial application of devices that take advantage of the different physical rules that apply to the atomic level.

One emerging nano resolution application, for instance, is the use of sub-wavelength optical components and photonic crystals in computers that process light, not electrons. Other applications include molecular electronics, biochemical analysis devices, high-speed compound semiconductor chips, distributed feedback lasers, high-density patterned magnetic storage media, and the directed self-assembly of carbon nanotubes.

To make all that a reality, we need to start making nano- scale objects with nanoscale tools. Once we begin doing that, the nanotechnology age will have arrived.

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