Reprint of

"S-FIL™ for Sub-80nm Contact Hole Patterning"

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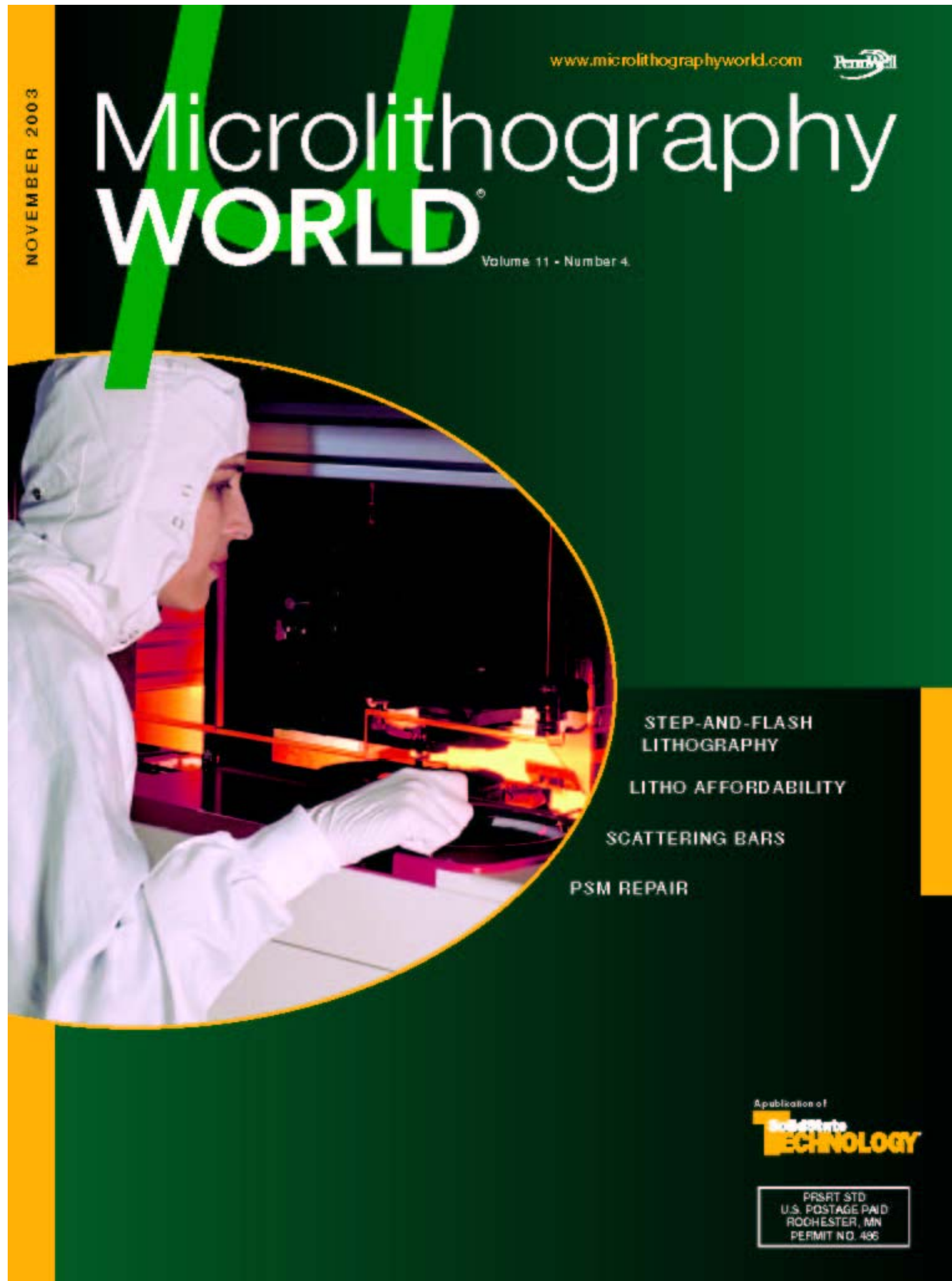

Cover photo courtesy of Molecular Imprints, Inc.

Cover Photo: An engineer looks inside the Imprio™ 50, a sub-50nm lithography tool with Step-and-Flash imprint lithography technology that delivers high resolution capability and 3-dimensional replication. It handles up to 8-in. wafers, including fragile substrates, and has a 10 x 10mm active print area.

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S-FIL™ for sub-80nm contact hole patterning

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Reliable printing of sub-80nm contact holes is a challenge that manufacturers of state-of-the-art DRAM and MPU devices must overcome within the next few years. Step-and-flash imprint lithography (S-FIL) has already demonstrated the ability to resolve sub-30nm lines in previous studies. Here, the first commercially available step-and-repeat imprint tool is used to demonstrate the ability of S-FIL to repeatably print dense arrays of sub-80nm contact holes.

Currently, 193nm lithography is being integrated into production fabs around the world to manufacture state-of-the-art silicon devices. At the same time, however, the future of lithography beyond the 193 horizon is not at all clear. What technology will establish itself as the heir apparent to 193? Immersion lithography applied at 193nm, 157nm lithography, and extreme ultraviolet lithography (EUVL) each promise to extend current capabilities and enable continued advancement in IC performance. However, immersion lithography is still in the early stages of development, and the time for introduction of EUVL is still several years away. In recent months, even the future of 157nm lithography has had considerable doubt cast upon it by Intel's announced decision not to install this technology in any of its fabs.

The International Technology Roadmap for Semiconductors (ITRS) has outlined concrete goals for critical dimensions (CD) needed to maintain the advancement of memory and microprocessor units (MPU). The schedule defined by ITRS for contact holes is quite

aggressive. For 2003, ITRS calls for a contact-hole CD in resist of 122nm and only 75nm by 2007. Due to their shape and the poor aerial image created in projection lithography, contact holes by nature are difficult to resolve. In addition, trim etches routinely used to further reduce the CD of gate resist lines cannot be applied to contact holes. As a result, nanoimprint technology, with its inherent independence from aerial image constraints, may become an important option for meeting this challenge.

Several nanoimprinting techniques are being actively developed as alternative approaches to optical nanolithography. Imprint lithography is essentially a micromolding process in which the topography of a template defines the patterns created on a substrate. Investigations by Motorola Labs and others have shown that the resolving potential of imprint lithography is only limited by the resolution of the template fabrication process [1–5]. These techniques possess important advantages over photolithography and other next-generation lithography (NGL) techniques since they do not require expensive projection optics, advanced illumination sources, or specialized resist materials. As a result, nanoimprint lithography has the potential to offer a significant cost-of-ownership reduction when compared to other NGL methods such as EUVL [6].

Step-and-flash imprint lithography

Invented at the University of Texas at Austin [7], S-FIL is one of the new methods of nanoimprint lithography being actively developed. As with other nanoimprint methods, S-FIL has been shown to be capable of sub-30nm resolution [4]. The process, depicted in Fig. 1, uses a transparent template containing the pattern to be printed etched into its surface:

a) Using a precise piezo-driven dispense head, a silicon-rich, low viscosity, photocurable, monomer solution is dispensed onto the substrate in the region where the pattern is to be printed.

b) The template is then pressed into contact with the wafer using very low pressures (1psi) to spread the liquid across the field and fill the template's relief.

c) UV light is irradiated through the back of the template, curing the monomer.

d) The template, pre-coated with a fluorocarbon release agent, is removed, leaving the cured, patterned resist layer behind.

e) Finally, a breakthrough etch passing through residual etch barrier and a transfer layer (any organic spin-coated resin such as an antireflective coating, ARC) transfers the high aspect ratio pattern to the substrate.

Many challenges remain ahead before S-FIL can be considered for integration into any type of manufacturing environment. These challenges result from two factors common to all imprinting lithographies: 1) each has a basis in contact printing (although for S-FIL, a key difference is that a low-viscosity liquid is present between template and wafer, creating a "lubricated" process), and 2) each uses masks (templates) that are sized at 1x. With contact printing comes the potential to generate and propagate defects. Therefore, the durability for printing thousands of defect-free die without template cleaning or maintenance must be demonstrated. In addition, overlay and distortion correction issues

must be solved for a transparent template.

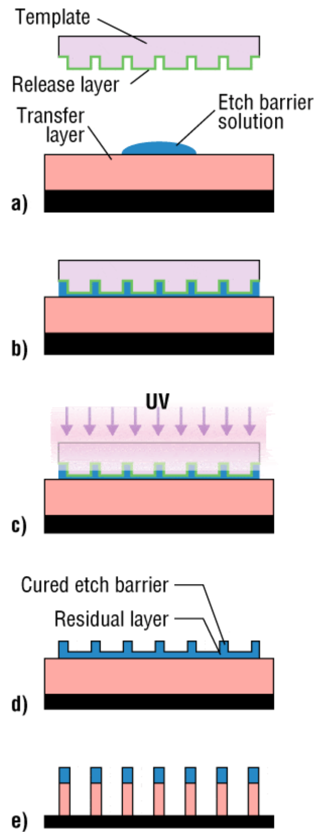

Figure 1. Process flow for step-and-flash imprint lithography [8]. The silicon-containing etch barrier monomer is applied in a) and the cured barrier layer is used as mask for etching in e).

However, it is likely that the mask industry itself would feel the greatest effect. Any move toward a 1x-based lithography will accentuate the need for fast writing, high resolution, pattern generation capable of extremes in both pattern placement accuracy and CD control. Additionally, an entirely new emphasis on cleaning, inspection, and repair of templates would be required since, in imprint lithography, there is no analogy to pellicles. In short, a whole new level in maskmaking infrastructure would need to be established.

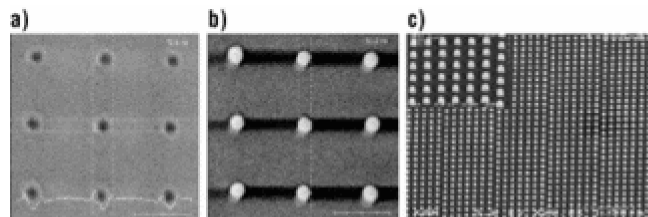

Figure 2. a) Template resist image of 80nm design pillars, pitch 1:2, actual CD = 72nm; b) finished template image of 80nm design quartz pillars, pitch 1:2, actual CD = 51.2nm; c) finished template image of 80nm, 1:1 pitch pillars following 20 consecutive wafer prints (740 die).

S-FIL template fabrication

The fabrication methodology used for S-FIL templates is similar to that used to manufacture phase-shift masks. A chromium film 15nm thick is first sputtered onto a standard 6 x 6 x 0.25 in. (6025) quartz mask blank. The plate is then coated with ZEP 520A positive e-beam resist, and exposed using a Leica VB6 electron-beam exposure system operating with a beam accelerating voltage of 100keV. Following development, the resist mask is used to pattern the chrome layer, after which it is stripped in a piranha bath. The chromium layer is next used as a hard mask to etch into the quartz substrate to a depth of ~100nm. The chrome layer is stripped, leaving an all-quartz template. Finally, the active printing area (a 25 x 25mm square) is formed into a pedestal by etching back the surrounding region using a separate patterning step and a timed, wet hydrofluoric acid etch. Templates are diced from the 6025 blank quartz plate to their final external dimensions of 65 x 65mm using a diamond saw.

Printing contact holes using S-FIL requires an array of pillars — a worst-case structure from the point of view of template wear — to be fabricated on the template. ZEP 520A resist offers extremely high contrast for this task, enabling pillars with as much as a 4:1 aspect ratio (Fig. 2a) to be resolved. However, two factors make achieving sub-100nm target CDs especially challenging: Proximity effects are significant, and so the pillar CD depends strongly on the designed pitch. For a given exposure dose, as the pitch increases (space between pillars widens), the resulting pillars are biased smaller. Complicating matters further, the development of features smaller than 100nm is highly nonlinear with dose, and so a pillar array can be completely cleared by only a slight over-exposure. Figures 2a and b show an array of pillars with a 80nm design size and a 1:2 pitch a) after resist develop and b) for the final template. The resulting pillars measure only 72nm due largely to proximity effects. Figure 2c shows a defect-free array of 80nm pillars having a pitch of 1:1 imaged after 20 wafer prints (740 die).

Wafer prints

All imprinting was done on 200mm silicon wafers using an Imprio 100 system manufactured by Molecular Imprints Inc. (MII), Austin, TX. Prior to imprinting, wafers were coated with a 600Å planarizing layer of Brewer Science DUV30J ARC. MII cleaned and coated the template with a fluorocarbon release material using a proprietary process. For these tests, 10 wafers were run consecutively with 37 fields printed on each wafer. During the tests the template was not cleaned or altered in any way, or removed from its chuck. Figure 3a shows a printed array of contact holes measuring approximately 66nm dia. This array was the result of a pillar array on the template designed at 80nm with 1:1 pitch. A bias of about 7–10nm between pillar and printed contact was measured, which may be a result of some sloping of pillar sidewalls. Figure 3b was taken on the 10th wafer of a consecutive series of prints. This field, the 370th in the series printed, shows no discernable degradation compared to 3a, which was imaged from the first wafer printed. Before this experiment, there was considerable concern about the fragile nature of sub-100nm pillars having an aspect ratio in excess of 1.0. It was not known whether these structures would withstand the shearing forces, however minute, they may encounter during the printing and releasing process. The tests did much to allay these fears, showing both the robustness of the template and the gentle nature of the printing

process.

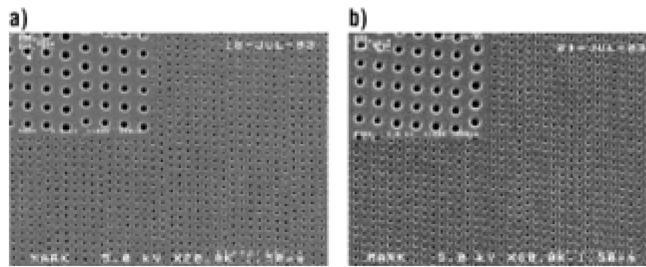

Figure 3. 80nm design contact hole array, 1:1 pitch, CD = 66nm: a) wafer #1 of 10-wafer series; b) wafer #10.

Figure 4 depicts cross-sectional SEM micrographs of printed contacts in the etch barrier layer. Figure 4a shows contacts created by a 100nm (1:1 pitch) template pillar array, measuring 89nm at the top and approximately 60nm at the bottom, reflective of the slope in template sidewalls. Figure 4b shows contacts created by an 80nm (1:2 pitch) template pillar array, measuring 72nm at the top and approximately 49nm at the bottom. Completion of this process with transfer of contact holes down to the substrate will require both a breakthrough etch of the residual layer and a transfer layer etch. Work on these etch processes is proceeding at the U. of Texas at Austin and at Motorola Labs [9].

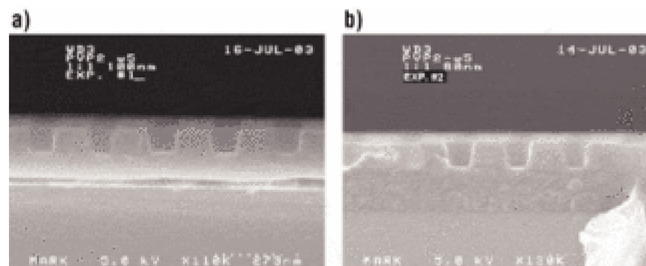

Figure 4. a) Cross-sectional SEM of 100nm contact holes, pitch = 1:1, top CD = 89nm; b) cross-sectional SEM of 80nm contact holes, pitch = 1:1, top CD = 72nm.

Conclusion

Step-and-flash imprint lithography has made considerable progress in a very short time, overcoming many important technical hurdles along the way. The first commercial step-and-repeat imprint tool has shown the ability to print sub-80nm contact hole arrays. No apparent degradation in printing quality was noted following almost 400 consecutive imprints. Given the inherent difficulty of printing contacts using optical methods, it may turn out that a nanoimprint method such as S-FIL may be called upon to meet this challenge. Achieving success will require a combined effort not only from S-FIL processing and tooling engineers, but from mask fabricators as well. Producing high-quality 1x templates for S-FIL will be, without question, a considerable challenge for the mask industry in the era of sub-100nm linewidths. However, it seems assured that mask production will be dramatically more difficult for fabricators and more costly for users regardless of which NGL technology is ultimately adopted.

Acknowledgments

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