



Imprinting the future of lithography

New credibility comes with inclusion in road map

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With its inclusion in the International Technology Roadmap for Semiconductors (ITRS) last month, imprint lithography gained credence as a potential successor to optical lithography in the fabrication of silicon chips. That being true, however, the technology still has hurdles, both technical and psychological, to cross. And when it comes to optical lithography, the Methuselah of process technology, one should never bet the farm—or the fab—against it.

In the simplest of terms, imprint lithography is just that: physically imprinting a resist on a substrate and creating features through subsequent process steps. Nanoimprinting, a term more and more associated with imprint litho, means doing it on a nanometer scale, a nanometer being one billionth of a meter. The technology is drawing increasing interest for—and is already beginning to be utilized in—several applications, ranging from biotechnology to microfluidics, MEMS, magnetic storage and optoelectronics. That list doesn't even include semiconductors.

The technology has actually been around for some time and exists in several iterations. The technology most likely to lend itself to semiconductor processing involves the curing of an imprinted polymer on top of a silicon substrate at room temperature and pressures, using ultraviolet light. Currently several equipment companies are involved in various kinds of imprint technology, including this UV curing approach.

The relative simplicity of imprint lithography and its potentially cost-effective application appeal to chip makers, particularly in light of the rising cost and complexity of extending optical lithography or developing and implementing a successor, such as extreme-ultraviolet technology. Suppliers of imprint tools estimate that eventual production tool sets may cost a 10th to a 50th as much as today's optical exposure tools. **Motorola**, in particular, is one chip maker closely involved in imprint research and development. The latest vote in this technology's favor was last month's official recognition of imprint litho by the industry consortium responsible for the ITRS as a potential alternative to optical lithography at the 32-nanometer node.

For the engineers and management of startup **Molecular Imprints Inc.** (MII), inclusion of imprint technology in the ITRS was a personal triumph. MII was born at the University of Texas, where its particular version of UV-cured imprint lithography, step-and-flash imprint lithography, was developed. MII's cofounders, Grant Willson and S.V. Sreenivasan, along with Doug Resnick of Motorola and Neil Richardson of **KLA-Tencor**, an MII investor and strategic partner, were all directly involved in campaigning for imprint's inclusion in the ITRS.

Although imprint holds promise, the polymer is not cut and dried, so to speak. The technology's proponents readily admit that they will have to address defect and throughput issues, critical dimension control and the development of full-field templates, the equivalent of today's photomasks. Introduction of defects is of particular concern; the smaller the feature sizes get, the more particle defects have the potential to wreak havoc. With imprint litho, which involves physical contact between the wafer and template, particle defects are naturally a primary concern.

But none of these issues appear insurmountable, say suppliers. "Those are a lot of the questions that remain to be answered," acknowledges Norm Schumaker, CEO of MII. He observes that this is why the technology was placed at the 32-nm node in the ITRS road map. "But we think the capability exists today to make those feature sizes," he says.

But then imprint lithography may face more mental, as opposed to technical, roadblocks. The industry is nothing if not conservative, and the idea of physically touching a patterned wafer makes engineers nervous. But imprint could follow chemical mechanical planarization in this respect. Once anathema to chip makers, the grinding and polishing of a patterned wafer is now a common process step in advanced fabs, particularly on copper fab lines.

It will be a matter of continuing R&D and providing relative data on defect rates and throughput to convince chip makers of the efficacy of imprint lithography, according to Peter Podesser, CEO of Austrian process tool vendor **EV Group**. Just how and when imprint lithography will be implemented in chip fabs remains to be seen; both Schumaker and Podesser envision that imprint will coexist side by side with optical technology or its successor, each being utilized for layers where they prove most cost-effective.

But in the end, as Schumaker notes, it's best not to make predictions where optical litho is concerned. With its doom forecast time and again, it persists today, and the promise of immersion technology may extend the technology yet again further than anyone has dreamed. Only time and a lot of R&D will tell.