

## **Interview with Dr. Norman E. Schumaker NanoMagazine.com July 2005**

Questions by Sander Olson. Answers by Dr. Norman E. Schumaker

Dr. Norman E. Schumaker is the President and CEO of Molecular Imprints, an innovative lithography company. A 30 year veteran of semiconductor business operations and technical management experience. Norm previously founded EMCORE Corporation, a leading supplier of compound semiconductor fabrication equipment. In addition, he established nLine Corporation and managed the New Materials and Technology Group at AT&T Bell Laboratories.

### **Question 1: Tell us about yourself.**

I went to small school called Wabash College in Indiana. I received my PhD from MIT in physical chemistry. From there I went to Bell Labs at Murray Hill and stayed for about 16 years. I left Bell Labs in 1984 to start a company called EMCORE, which was making molecular chemical vapor deposition equipment for semiconductors. In 1996, just before EMCORE went public in early 1997, I left and moved to Austin and went looking for new technologies. At the University of Texas, I discovered the "step and flash" technique created by Drs. S.V. Sreenivasan and C. Grant Willson, which has become the foundation for Molecular Imprints.

### **Question 2: Tell us about Molecular Imprints.**

Molecular Imprints Inc (MII) ([www.molecularimprints.com](http://www.molecularimprints.com)) is a company that is focused on a new lithography that doesn't employ any optics or light, other than to cure materials. It is a high resolution "molding" technique developed by C. Grant Wilson and S. V. Sreenivasan. Grant Wilson perceived that very low viscosity liquids will fill tiny cavities, due to capillary forces. Wilson came up with the concept of using a quartz template, created by etching fine patterns into quartz, and using a low-viscosity liquid to fill the cavities etched into the surface of the template. If these materials are exposed to ultraviolet light, then they turn into polymers, and intricate patterns can be formed. If you like, imprinting is a high tech analogue to the wax stamp used to seal envelopes and documents.

This technique is capable of reproducing the minutest features. Researchers at the University of Illinois have actually replicated 2.2 nm carbon nanotubes structures using imprint lithography. With dimensions as small as 0.1 nanometer, we are in the realm of molecular dimensions.

### **Question 3: How long do you think that conventional lithography will be effective? Will imprint lithography be able to seriously challenge Extreme Ultraviolet Lithography (EUV)?**

Optical lithography is the major lithographic technique and will continue to be used for many applications. However as features become smaller, MII's imprint technique will see increasing use.

We are the dark horse in the next-generation lithography race, since we have a radically different way of making patterns. EUV, which is soft X-rays, will be employed exclusively for making silicon integrated circuits. Our technique, by contrast, can be used for a broad range of applications - everything from high-resolution filters in projection televisions, to LEDs, to patterned media for magnetic drives, to micro optics (which are used in projection televisions and solid-state cameras in cell phones) biomedical applications, and micro fluidics. This is in addition to the things that we can be doing with compound semiconductors and even silicon. We think that there may be applications in the silicon industry for specialized uses of imprint technology in areas where optical technology has great difficulty.

In my estimation, the market will make its choices, probably in the next couple of years, and it will be a competition between what we can do with imprint vs. what they can do with soft x-rays (EUV).

**Question 4: Has MII been able to create functional transistors using imprint lithography? Will we ever see volume production of 10 nm transistors?**

The University has already demonstrated transistors made by imprint technology as well as others. Creating large scale integrated circuits with imprint lithography is probably a couple of years away. We need to get technical insight from the device manufacturers before we can fabricate mask sets in order to make active devices. We need to make detailed demonstrations before we get to that point, which is probably 12-18 months out. But there are no "show-stoppers" or fundamental obstacles to making IC's with imprint lithography.

It is definitely possible for imprint lithography to create 10 nanometer transistors. If 10 nanometer transistors become viable for manufacture in volume, then imprint lithography will probably be the only way to do it. In terms of manufacturing volumes, I think that EUV is just going to be too expensive. Tools for EUV could cost in excess of \$50 million dollars a piece, and that isn't even taking into account all of the infrastructure that is needed to support the tool. The light sources for EUV are incredibly inefficient, and are very short-lived, and the cost of manufacturing using EUV could be prohibitive except for highly specialized applications. As the semiconductor industry continues down Moore's law's path, we will have increasing opportunities to sell tools for silicon application.

**Question 5: How does imprint lithography compare with x-ray or e-beam lithography?**

X-ray lithography has been worked on for a number of years, and I believe that there are still a few individuals researching that approach. The problem is that the x-ray lithography mask is actually a membrane, and therefore has certain mechanical and thermal limitations which limit its usefulness in a manufacturing environment. By contrast, our template is made from the same 6025 mask blank that the industry has been using for years. So while the concept of x-ray lithography is interesting, the industry is moving away from x-ray lithography as a contender for next-generation lithography.

The semiconductor industry has been using direct-write e-beam lithography for several years for early prototyping. We actually make our templates using e-beam lithography. It is an elegant technique with a high-resolution capability, but it is incredibly slow. As a consequence, the cost of ownership associated with using e-beam lithography in manufacturing is prohibitive. So while these technologies are interesting, I don't believe that either x-ray or e-beam technology will ever move into manufacturing.

**Question 6: How has MII prevented material from sticking to the template? How long before the template wears out?**

Keeping materials from sticking to a surface is really a chemistry problem. We have a small group of polymer chemists and material scientists who have been working on understanding the chemical and physical properties of quartz relative to the monomer solutions that we use in our process. We've worked out the chemistry such that materials do not stick to the template, and we have a "release layer" which keeps material from sticking to the template.

There is no contact in our process with the substrate, and as a consequence, there is no damage to the template other than potentially from particulate contamination from the atmosphere. We don't see any degradation of the template during the process so the lifetime of the template will be quite long. It is conceivable that you could have a very hard particle that could potentially

damage the template, but we have not seen that occur at all at this point. Actually, you may want to clean the template in the same fashion that people clean masks and pellicles, we've worked out the processes so that that can be done very efficiently.

**Question 7: How expensive is the equipment for imprint lithography? How much would a complete set appropriate for semiconductor lithography cost?**

People are usually surprised when they see how simple our process is. The tool is fundamentally simple and we actually dispense the liquid only in the amount that is actually needed so materials costs are attractive. We can actually process 4,000 200 mm wafers with only 10 milliliters of liquid. Also, we expect that the final template costs will be cost effective compared to current mask costs, so that overall our Cost of Ownership will be quite appealing.

The actual tools are dependent upon the application requirements. Our simple R&D tools are roughly \$500,000, our Development tools are roughly \$1,000,000, our pilot production tools are in the range of \$2 -5,000,000 and a full scale high precision manufacturing tool will be less than \$10,000,000. Tool prices of course, are dependent on the requirements demanded by the customer so we are flexible with our tool designs to allow the customer to select the most cost effective options for the particular application.

**Question 8: What sort of throughput does imprint lithography provide?**

We've been working at MII to systematically address all of the issues associated with using this technique in semiconductor manufacturing. First, we designed tools for research applications which allowed us to study and understand the behavior of the liquids which are an important part of the process. The second-generation tool that we have just recently released is focused on the providing the customer with very high-resolution alignment and overlay capability, and that tool is finished. That tool, the Imprio™ 250, has a throughput of five 200 mm wafers per hour, which is relatively slow compared to production tools, but which is sufficiently fast that people can begin to evaluate the tool for silicon type applications. It is also fast enough that it actually becomes a production tool for some of our emerging markets applications, which we are identifying.

The next-generation tool, which should become available in two years, will focus on high-throughput, and we think that we should be able to develop an imprint tool which will have wafer throughput on the order of 25 wafers per hour at 300 mm, and maybe substantially higher than that. That would make it compatible with manufacturing in silicon. Our customers generally believe that a throughput of 25 wafers per hour would be the minimal acceptable throughput. We hope to eventually succeed that by factors of two or four.

**Question 9: Have semiconductor makers such as Intel or IBM shown interest in imprint lithography?**

We have numerous non-disclosure agreements (NDAs) with many different companies, so our policy is not to discuss customers to whom we've sold tools or have active discussions unless we receive permission. I can assure you that we are talking with many silicon manufacturing people, who understand that our tool is not ready for large-scale manufacturing. I can safely say that these companies are watching us very closely, and are getting interested in testing the technology in conjunction with our becoming a potential vendor.

**Question 10: How many defects per square meter do you experience in your wafers?**

We are just in the early stages of starting our defect studies. Defects in semiconductor manufacturing are characterized by defects per wafer, as opposed to defects per square centimeter. Consequently, defect studies are inherently difficult and time consuming, since many

factors contribute to the presence of defects. Defects can potentially arise in the template fabrication technique, in the process of doing the imprint, or in the tool itself. So we are systematically working through the origins of defects in the patterns that we create. We have prepared wafers with about 25 defects per 200 mm wafer, but those are the best results of our tests so far. By the end of the year, we should have some compelling statistical data to show that our process is clean and not inherently defective. In other words, we don't create defects with the process. We are also, systematically eliminating sources of defects in the tool operations, and we are receiving a great deal of cooperation with the template makers, who are working diligently to help us understand where the defects arise in the fabrication of templates. We are confident that the template makers will be able to show that they do not produce defects in their template process.

However, we think that there are other areas besides integrated circuits which are not sensitive to defects for which imprint is well suited. For example, in compound semiconductor devices, where ICs are typically on the order of 1mm square, a 200 mm wafer can accommodate hundreds of 1mm square devices. In this case imprint lithography can provide substantial advantages, since a small number of defects will not substantially impact yields. In addition, to compound semiconductors there are many other applications for imprint lithography. We have been focusing attention on things like optical filters, gratings, and other averaging devices. Micro-lenslets for cameras and solid state lighting LED's are other potential markets for imprint technology.

We foresee a large market for our tools outside of silicon.

**Question 11: What are the plans of MII for the next decade? Do you see a thriving industry based on imprint lithography by 2015?**

It is difficult to project so far in advance, given that the company is only four years old. I'm very bullish on this technology. I'm as enthusiastic today as when I first saw the imprint technology at the University of Texas. I am very enthusiastic about the possibility of imprint technology being the technology of choice for high-resolution patterning being used in 10 years. I am absolutely certain that there will be consumer products, such as micro-optical components for use in projection televisions and cameras, which will be made by imprint lithography. This could happen within two years.