

Semi road map adds imprint, maskless lithography

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Austin, Texas - Maskless and imprint lithography have been added to the 2003 edition of the International Technology Roadmap for Semiconductors, swelling the options in the critical lithography arena.

The road map, rolled out last week at a meeting in Taiwan, adds a new designation-"litho-friendly design"-to emphasize the importance of avoiding forbidden pitches and other design no-no's.

Maskless lithography (see Sept. 22, page 18) goes on the road map at the 45-nanometer node, which could see early production in 2007. Imprint was added to the 32-nm node, coming in 2009, though realistically it may be 2013 before imprint lithography is ready for volume production, said Walt Trybula, a senior fellow at International Sematech, based here.

In the late '90s, Sematech sponsored several well-publicized next-generation lithography workshops, with votes taken among the 150 or so participants. Extreme-ultraviolet (EUV) lithography gradually gained favor, X-ray lithography was dropped as the challenge of making the proximity membrane masks became apparent and options were further whittled down to four serious next-generation lithography candidates. Despite that sorting out, however, 11 or 12 forms of maskless and masked lithography are now being seriously pursued, Trybula said.

The economics of going down many paths is so troubling that Sematech's executive steering committee has called for a Sematech-organized forum to reconsider the entire lithography question. It is planned for late next month in Los Angeles.

The variety of options is apparent from the 2003 edition of the Sematech road map, finalized last week at the Taipei meeting. At the 65-nm node, defined as the half-pitch of the line and space for DRAMs, exposures will be handled largely with 193-nm-wavelength scanners and masks with optical proximity correction, phase shifting and other reticle enhancement techniques.

In addition to "dry" 193-nm tools, immersion, or "wet," 193-nm scanners are expected to be ready in 2005 and could be used to enhance 248-nm scanners as well. For 65-nm devices, dry and wet (immersion) 193-nm tools, 157-nm scanners, the electron-beam projection lithography being developed by Nikon Corp., direct-write e-beam and another system being developed by Japan's low-energy e-beam proximity projection lithography (LEEPL) consortium all are on the 2003 road map.

Trybula said some companies, including STMicroelectronics, now use direct-write e-beam to create prototypes. These single-beam tools are slow and are not to be confused with the multibeam tools being developed for maskless lithography, which would handle five or more wafers per hour. Maskless has another flavor as well,

based on micromirrors for optical modulation of light directly on the wafer without an intervening mask (see Sept. 8, page 1).

Maskless lithography is being spurred in part by the needs of ASIC manufacturers. Trybula, citing data provided to Sematech by LSI Logic Corp., said the average ASIC mask set processes only six wafers. Semiconductor foundries also have many small-volume runners and are backing maskless lithography, known as ML2.

Two forms of lithography were taken off the 2003 road map: ion projection, backed by Infineon Technologies, and proximity X-ray lithography. Trybula said six companies, including several in Japan, continue to offer X-ray lithography for prototype or test chips, gallium arsenide designs, military-use semiconductors and other "specialty" apps. JMAR Technologies Inc. (San Diego), with funding from the Pentagon, also is developing a form of X-ray lithography that it offers to commercial IC vendors for the critical dimensions.

Trybula said EUV lithography, which uses reflective optics and masks to bounce 13.5-nm-wavelength light onto a wafer, goes on the road map for introduction at the 45-nm node.

The issue of line-edge roughness of the developed resists is getting more attention, Trybula said. Chemical amplification techniques in resists may become less effective as scaling proceeds. "LWR [line-width roughness] is becoming a concern, and experts such as Grant Willson [a University of Texas professor and former IBM resist scientist] are saying that we may have to decrease the amount of amplification to deal with LWR. But the resist companies are working on it," Trybula said.

Adding imprint lithography to the road map is intriguing from a cost perspective, because imprint systems do not require the sophisticated optics of conventional scanners, which reduce the image on a mask by four times with either projection or reflection optics. Imprint lithography uses polymers that harden into patterns when exposed to ultraviolet light through a template. The template is a 1:1 proximity mask-the pattern on the template is at the same dimensions as the finished product, rather than at the 4x reduction.

Princeton University-backed Nanonex Corp. (Princeton, N.J.) has shipped an imprint lithography tool to the University of Michigan, among other customers.

In Europe, a maker of scanning electron microscopes, Obducat AB (Malmo, Sweden), has shipped dozens of imprint tools, some of which expose patterns for disk drive heads.

Molecular Imprints Inc. (MII), a spin-out from the University of Texas (Austin), has worked with Motorola Inc.'s corporate research lab in Tempe, Ariz., to develop the imprint templates. Norm Shumaker, MII's president and CEO, said the company has shipped three of its Imprio 100 lithographic tools, one to Motorola's Tempe lab, one to the Korea Advanced Institute of Science and Technology and a third to a large Silicon Valley-based electronics company. He would not name the company but said it was not Intel Corp. The Imprio 100 sells for about \$1.5 million. MII also is selling less-expensive systems that lack alignment capabilities.

MII recently closed on \$15 million of second-round financing, most of it going to roughly double today's staff of 35 and to develop in 2004 a next-generation tool with more advanced alignment control.

Critical levels

On the technical front, MII's goal is for its imprint systems to be used for one or two of the critical mask levels at the 65-nm or 45-nm node—perhaps the poly gate formation layer that is crucial to microprocessor manufacturers.

One challenge facing imprint lithography is that the mask, called a template, must be scribed at 1x the pattern dimensions. The "1x" mask challenge was largely responsible for sinking prospects for X-ray lithography, though X-ray continues to be developed for specialty applications. One key difference, Trybula said, is that X-ray masks must include a thin membrane on top, which is difficult to make. Imprint templates are more straightforward to manufacture.

MII's co-founder, S.V. Sreenivasan, said the optical-mask manufacturers are becoming more comfortable creating 1x patterns, in part because they are used increasingly for optical phase shift and optical proximity correction masks. Also, an imprint template is much smaller than the reduction optical masks. Sreenivasan argued that a 4x "highly decorated" mask with extensive optical proximity correction could cost much more than an imprint template, largely because the scribed pattern is much smaller in total area.

"The mask makers already are doing 1x patterns, and that is helping us," Sreenivasan said.